REMARKS

Claims 5, 6, 7, 16 and 17 are pending in the application. By this amendment, claim 16 is being amended so as to clearly distinguish patentably over the prior art, and claim 17 is being amended to improve its form; marked up versions of the amended claims are attached hereto pursuant to 37 C.F.R. § 1.121(c)(ii). No new matter is involved. Entry of the amendment under the provision of 37 CFR § 1.116 as placing the application in condition for allowance or alternatively in better form for appeal, and reconsideration and allowance in view thereof, are respectfully requested.

On page 2 of the Office Action, claims 16, 5 and 6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,962,890 of Sato in view of JP 407161848 of Mori. At the top of page 5 of the Office Action, claim 7 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Sato in view of Mori, and further in view of U.S. Patent 5,907,171 of Santin et al. In the middle of page 5 of the Office Action, claim 17 is said to be allowed.

Shortly prior to issuance of the final Office Action of December 28, 2001, Examiner Tran telephoned the undersigned to state that he had reviewed applicant's Amendment of September 12, 2001, and in view thereof was allowing claim 17. The Examiner stated that claim 16 would probably be allowable if limitations similar to those set forth in the last two paragraphs of claim 17 were added thereto. The Examiner referred to newly uncovered U.S. Patent 5,962,890 of Sato, and specifically to Fig. 3 of Sato as showing that the isolating region defined

in claim 16 is known in the art. Unfortunately, applicant was unable to respond to the Examiner's proposal before the Examiner had to act on the application, and this resulted in issuance of the Final Office Action on December 28, 2001.

In response to the telephone call from the Examiner and to the Final Office Action, applicant is amending claim 16 in the manner suggested by the Examiner. More specifically, claim 16 is being amended to add at the end thereof the recitation "in each of said memory transistors, both said oxide film and another oxide film are formed between each said side wall and each of said floating and control gates, and are formed between each said side wall and said substrate", and the further recitation "in each of said element separating regions, both said oxide film and said another oxide film are formed between each said side wall and each of said control gates, and only said another oxide film is formed between each said side wall and each element separating insulating film". As so amended, claim 16 is similar to allowed claim 17, and clearly distinguishes patentably over the attempted combination of Sato and Mori as set forth in the final Office Action.

Claims 5 and 7 depend from claim 16, and claim 6 depends from claim 5. In view of the amendment herein of claim 16, these claims are also submitted to clearly distinguish patentably over the prior art.

Claim 17 has been allowed. At the same time, applicant is amending claim 17 herein in order to make minor amendments to the last two paragraphs thereof in order to grammatically improve the claim without in any way changing the substance of the claim.

In conclusion, claims 5-7 and 16 are now submitted to be in condition for allowance in addition to claim 17. Entry of the Amendment under 37 CFR § 1.116 as placing the application in condition for allowance or alternatively in better form for appeal, and reconsideration and allowance in view thereof, are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles telephone number (213) 337-6846 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,

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Date: February 25, 2002

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Version with markings to show changes made:

IN THE CLAIMS:

Rewrite claim 16 as follows:

16. (Twice Amended) A nonvolatile semiconductor memory device comprising:

a semiconductor substrate;

memory transistors formed on said semiconductor substrate to perform nonvolatile storage of an electric charge in accordance with data, each of said memory transistors being an electrically rewritable memory transistor including a floating gate formed over said semiconductor substrate via a first gate insulating film and a control gate formed over said floating gate via a second gate insulating film;

an oxide film formed on said substrate and at least on both sides of each said floating gate and both sides of each said control gate;

side walls each for protecting sides of said floating gate and said control gate of each said transistor, each said side wall formed from a first silicon nitride film formed by low-pressure CVD over said oxide film;

a second silicon nitride film covering surfaces of said control gate, a source diffusion layer, a drain diffusion layer and each of said side walls of each of said memory transistors and on surfaces;

a wiring layer formed over said second silicon nitride film via an inter-layer insulating film; and

element separating regions extending along one direction; and wherein

groups of said memory transistors are arranged along said one direction and adjacent said element separating regions;

in each of said element separating regions, an element separating insulating film is formed on said substrate extending in said one direction;

each of said floating gates is formed on each of said memory transistors between and to the exclusion of most of said element separating regions; [and]

said control gates extending in a direction perpendicular to said one direction and intersecting said memory transistors and said element separating regions, each said control gate being arranged on said element-separating insulating films in said element separating regions[.];

in each of said memory transistors, both said oxide film and another oxide film are formed between each said side wall and each of said floating and control gates, and are formed between each said side wall and said substrate; and

in each of said element separating regions, both said oxide film and said another oxide film are formed between each said side wall and each of said control gates, and only said another oxide film is formed between each said side wall and each element separating insulating film.

Rewrite claim 17 as follows:

17. (Three Times Amended) A nonvolatile semiconductor memory device comprising:

a semiconductor substrate;

memory transistors formed on said semiconductor substrate to perform nonvolatile storage of an electric charge in accordance with data, each of said memory transistors being an electrically rewritable memory transistor including a floating gate formed over said semiconductor substrate via a first gate insulating film and a control gate formed over said floating gate via a second gate insulating film;

an oxide film formed on said substrate and at least on both sides of each said floating gate and both sides of each said control gate;

side walls each for protecting sides of said floating gate and said control gate of each said transistor, each said side wall formed from a first silicon nitride film formed by low-pressure CVD over said oxide film;

a second silicon nitride film covering surfaces of said control gate, a source diffusion layer, a drain diffusion layer and each of said side walls of each of said memory transistors and on surfaces;

a wiring layer formed over said second silicon nitride film via an inter-layer insulating film; and

element separating regions extending along one direction, wherein

groups of said memory transistors are arranged along said one direction and adjacent said element separating regions;

in each of said element separating regions, an element separating insulating film is formed on said substrate extending in said one direction;

each of said floating gates is formed on each of said memory transistors between and to the exclusion of most of said element separating regions;

said control gates extending in a direction perpendicular to said one direction and intersecting said memory transistors and said element separating regions, each said control gate being arranged on said element-separating insulating films in said element separating regions;

in each of said memory [transistor] transistors, both said oxide film and another oxide film are formed between each said side wall and each of said floating and control gates, and are formed between each said side wall and said substrate; and

in each of said element separating [region] regions, both said oxide film and said another oxide film are formed between each said side wall and each of said control gates, and only said another oxide film is formed between each said side wall and each element separating insulating film.